Record-Performance In_2O_3 FETs with Ultra-scaled Contacted Gate Pitch: Enabled by Higher-*k* HZO Linear Dielectric and Novel Ti-Seeded Contact

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Abstract: In this work, we demonstrate two strategies to enhance the performance of oxide semiconductor (OS) FETs with ultra-scaled contacted gate pitch (CGP ≤ 80 nm). First, the gate capacitance-equivalent thickness (CET) is scaled to 1.36 nm using $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based linear dielectric with k > 28. Second, a novel ultrathin 0.5-nm Ti-seeding layer is introduced to further reduce contact resistance (R_C). By combining CET scaling and Ti-seeded metal contact, In_2O_3 FETs achieve a record-low R_C of 29.4 Ω·μm (approaching the Landauer limit), a record-high maximum current of 4.15 mA/μm, and a record-high on-current of 1.74 mA/μm among all reported OS FETs with contact length scaling. These results establish a new benchmark for OS FETs with ultra-scaled device footprints.

Introduction: In_2O_3-based oxide semiconductor (OS) FETs have attracted significant interests for monolithic three-dimensional integration (M3DI) [1, 2]. To date, substantial efforts have focused on channel length (L_{ch}) scaling to enhance OS FET performance and meanwhile reduce device footprint [3–14]. However, device footprint reduction is governed not only by L_{ch} but also by contact length (L_C), as both contribute to the contacted gate pitch (CGP), one of the metrics for device size [**Fig. 1(a)** and **(b)**]. Despite its importance, L_C scaling in OS FETs has been relatively underexplored [15–20]. When L_C is scaled to < 50 nm, pronounced performance degradation is commonly observed due to the current-crowding effect (CCE), where contact resistance (R_C) increases sharply once L_C < transfer length (L_T). This limitation highlights the need for further optimization strategies to fully realize the intrinsic performance potential of OS FETs in the ultra-scaled L_C < 50 nm regime. **In this work,** we explore two approaches to optimize In_2O_3 FETs performance with L_C < 50 nm. First, we scale the gate capacitance-equivalent thickness (CET) down to 1.36 nm using a $Hf_{0.5}Zr_{0.5}O_2/Al_2O_3/Hf_{0.5}Zr_{0.5}O_2$ (HZAHZO) gate dielectric with a higher-*k* value (k > 28) than conventional high-*k* HfO_2 (k ≤ 18) [3, 8, 9]. Second, we introduce a novel ultrathin 0.5-nm Ti-seeding layer at the Ni/In_2O_3 interface to reduce contact resistivity through moderated contact doping. By combining CET scaling and contact engineering, we demonstrate a record-low R_C of 29.4 Ω·μm approaching the Landauer (quantum) limit, a record-high maximum current (I_{max}) of 4.15 mA/μm, and a record-high on-current (I_{ON}) of 1.74 mA/μm among all reported OS FETs with L_C scaling. Highlights of this work are summarized in **Fig. 1(c)**.

Experiments: **Fig. 2(a)** shows the fabrication flow of the devices in this work. 40 nm W was sputtered as the back-gate, followed by the deposition of HZAHZO gate dielectric using plasma-enhanced atomic layer deposition (PE-ALD). To enable CET scaling, the total oxide thickness (T_{OX}) of the HZAHZO was varied from 12 to 8 nm [**Fig. 2(b)**]. Achieving a HZAHZO stack with higher k > 28 requires an asymmetric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) configuration, in which the bottom HZO layer (t_3) is thicker than the top HZO layer (t_1), with an intermediate Al_2O_3 layer (t_2) inserted to decouple the two HZO layers [7]. This asymmetric structure promotes the formation of tetragonal (t-) phase HZO with higher k through a favorable strain gradient from the bottom W electrode toward the top In_2O_3 capping layer [7]. The Al_2O_3 interlayer is applied to suppress the formation of ferroelectric phase. An ultrathin In_2O_3 with channel thickness (T_{ch}) of 1.8 –2.2 nm was subsequently deposited by ALD, followed by an O_2 annealing at 350 °C to form and stabilize the t-phase HZO. Device isolation and channel width definition were achieved using Ar dry etching. Source/drain (S/D) contacts were formed by in-situ e-beam evaporation of a 0.5-nm Ti-seeding layer at a rate of 0.01 nm/s, followed by 20 nm of Ni at a base pressure of ~ 4×10^{-8} Torr. The role of the ultrathin Ti-seeding layer in contact properties will be discussed later. **Fig. 3(a)** demonstrates a cross-sectional scanning transmission electron microscopy image of an In_2O_3 FET with ultra-scaled CGP of 70 nm.

CET Scaling: **Fig. 4(b)** shows the capacitance characteristics of HZAHZO gate dielectric. As the T_{OX} is reduced from 12 to 10 nm, the CET scales from 1.61 nm to 1.36 nm [**Fig. 4(c)**] while maintaining a k ≥ 28.6 [**Fig. 4(d)**]. However, further reducing T_{OX} to 8 nm leads to a CET increase accompanied by a degraded k value of 20.4 [**Fig. 4(c)** and **(d)**], suggesting a part transition from higher-*k* t-phase to lower-k monoclinic (m-) phase HZO [7]. The impact of CET scaling on In_2O_3 FETs performance is evaluated in **Fig. 5**. With CET scaled from 1.61 to 1.36 nm (T_{OX} = 12 to 10 nm), In_2O_3 FETs exhibit clear enhancements in field-effect mobility (μ_{FE}) [**Fig. 5(b)**] and I_D [**Fig. 5(a)** and **(c)**], underscoring the critical role of CET scaling in improving transistor performance.

L_C Scaling (from 500 to 40 nm): L_C scaling is investigated for devices with the minimum CET = 1.36 nm (T_{OX} = 10 nm) in this work. The impact of L_C scaling on short-channel transistors (L_{ch} = 50 nm) is illustrated by the I_D–V_{GS} curves in **Fig. 6(a)** and **(b)** for different T_{ch}. As L_C reduces, I_D [**Fig. 6(a)** and **(b)**], peak transconductance ($g_{m,peak}$) [**Fig. 6(c)**], and μ_{FE} [**Fig. 6(d)**] degrade, primarily due to the increase in R_C caused by the CCE. To quantify the impact of CCE on R_C, the transfer length method (TLM) is employed to extract R_C as a function of L_C, as shown in **Fig. 7(a)** and **(b)**. Extracted R_C–L_C characteristics are summarized in **Fig. 7(c)** and analyzed using the CCE model on planar devices [21]:

$$R_C = R_{C0}\, coth(L_C/L_T) \quad (1)$$

$$R_{C0} = \sqrt{\rho_C R_{sh}};\ L_T = \sqrt{\rho_C/R_{sh}};\ \rho_C = R_{C0} \cdot L_T \quad (2)$$

where R_{C0}, ρ_C, and R_{sh} represent R_C at $L_C \gg L_T$, contact resistivity, and sheet resistance, respectively. The extracted contact parameters are presented in **Fig. 7(d)**. Increasing T_{ch} leads to improved contact properties, with R_{C0} reduced from 38 to 33 Ω·μm, L_T lowered from 55 to 42 nm, and ρ_C decreased from 2.1×10^{-8} to 1.4×10^{-8} Ω·cm^2. These T_{ch} dependent contact properties are attributed to the quantum-confinement-controlled Schottky barrier height (Φ_{SB}) at metal/In_2O_3 interface, consistent with our prior studies [18, 19, 22]. R_C and R_{sh} as a function of overdrive voltage ($V_{OV} = V_{GS} - V_T$, where V_T is the threshold voltage) at ultra-scaled L_C = 40 nm are further examined in **Fig. 8(a)** and **(b)**. **Fig. 8(c)** benchmarks R_C versus 2D carrier density (n_{2D}) against the reported OS FETs with low contact resistivity. This work achieves a record-low R_C of 29.4 Ω·μm (extracted at 300 K) among all OS FETs with L_C < 50 nm, approaching even the lowest R_C reported in devices with L_C > 1 μm (23.4 Ω·μm extracted at 10 K [6]) as well as the Landauer limit shown in **Fig. 8(c)**.

Mechanism of Ti-Seeding Layer: The record-low R_C can be attributed to the introduction of an ultrathin 0.5-nm Ti-seeding layer at the Ni/In_2O_3 contact interface [**Fig. 3(b)**]. When Ti is deposited on In_2O_3, it induces oxygen scavenging reaction (OSR), in which Ti extracts oxygen from In_2O_3 due to its lower oxygen interstitial formation energy compared with indium [23]. This process generates oxygen vacancies (V_O^+) and locally increases the electron density beneath the S/D regions, analogous to n^+ contact doping in conventional *n*-type MOSFETs [**Fig. 9(a)**] [23]. Such n^+ contact doping is beneficial for the reduction of ρ_C. However, when a relatively thick Ti layer (>1 nm) is used, excessive OSR leads to the formation of a thick TiO_X interfacial layer that acts as a tunneling barrier, offsetting the benefit of n^+ contact doping and resulting in degraded ρ_C [23, 24]. In contrast, the ultrathin 0.5-nm Ti-seeding layer adopted in this work is optimized and enables a moderated OSR, providing sufficient n^+ contact doping to significantly reduce ρ_C while suppressing TiO_X formation to a thickness that does not degrade contact properties, as illustrated in **Fig. 9(b)**. As a result, the n^+ contact doping benefit can be effectively exploited. **Fig. 9(c)** compares the ρ_C of In_2O_3 FETs with conventional Ni contacts (our prior work) [18] and those with Ti-seeding layer + Ni contacts in this work, demonstrating a 73% reduction in ρ_C and corroborating the essential role of the ultrathin Ti-seeding layer in enabling low R_C.

Performance in Ultra-scaled CGP: **Fig. 10(a)** and **(b)** show the transfer curves of In_2O_3 FETs with ultra-scaled CGP ≤ 80 nm for T_{ch} = 1.8 nm and 2.0 nm, respectively. The corresponding output characteristics are presented in **Fig. 10(c)** and **(d)**. Enabled by strong electrostatic control from the higher-*k* HZAHZO and the record-low R_C, our devices achieve outstanding performance, as summarized in **Fig. 11**: a record-high I_{max} = 4.15 mA/μm [**Fig. 11(a)**] and a record-high I_{ON} =1.74 mA/μm [**Fig. 11(b)**] among all OS FETs with L_C scaling, while maintaining a subthreshold swing (SS) below 72 mV/dec [**Fig. 11(c)**].

Conclusion: This work employs two key strategies—CET scaling by HZAHZO higher-*k* dielectric and a novel 0.5-nm Ti-seeded contact—to enhance OS FET performance in the ultra-scaled L_C < 50 nm regime. Through these combined optimizations, our In_2O_3 FETs demonstrate record-low R_C and record-high performance among all reported OS FETs with L_C scaling.

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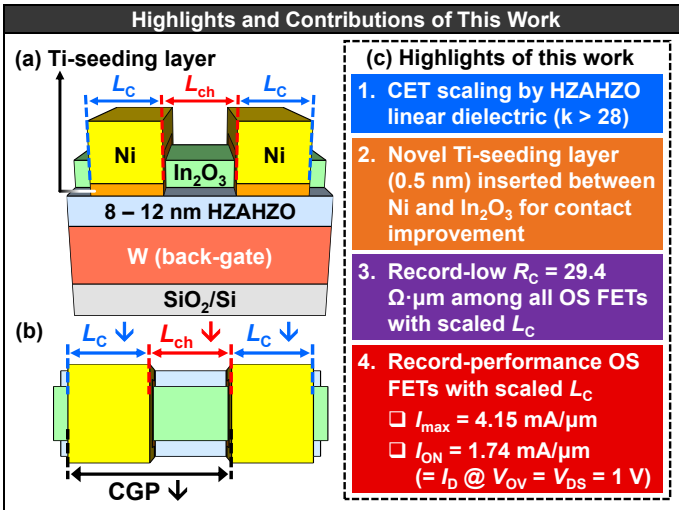

Fig. 1. Schematic device structure of an In_2O_3 FET: **(a)** three-dimensional view and **(b)** top view, where the CGP is defined as $L_C + L_{ch}$. **(c)** Highlights of this work. I_{ON} is defined as the I_D at $V_{GS} - V_T = V_{OV} = V_{DS} = 1$ V. Threshold voltage (V_T) is extracted by constant-current method at $I_D/W_{ch} = 100$ nA/L_{ch}. V_{OV} denotes the overdrive voltage, and W_{ch} is the channel width.

Fig. 2. **(a)** Fabrication process flow of In_2O_3 FETs with HZAHZO higher-k linear gate dielectric and novel Ti-seeded Ni contact. **(b)** Structure and thickness design of the HZAHZO stack investigated in this work. The underlying design rationale of the HZAHZO stack, including the use of $t_3 > t_1$, has been comprehensively studied in our previous work [7].

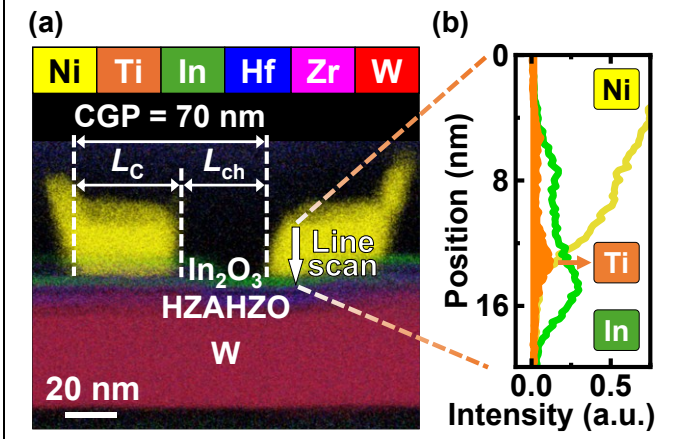

Fig. 3. **(a)** Cross-sectional scanning transmission electron microscopy (STEM) image with energy-dispersive X-ray spectroscopy (EDS) elemental mapping (Ni, Ti, In, Hf, Zr, and W) of an In_2O_3 FET featuring an ultra-scaled L_C of 40 nm and L_{ch} of 30 nm, corresponding to a CGP = $L_C + L_{ch}$ of 70 nm. **(b)** Elemental line scan along the arrow indicated in **(a)**, confirming the presence of the ultrathin 0.5-nm Ti-seeding layer.

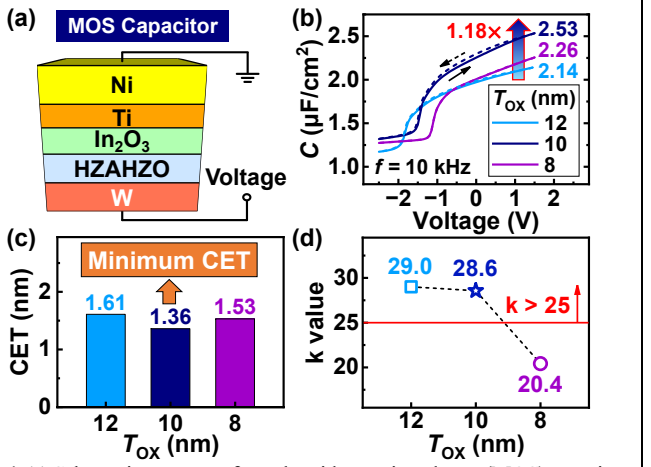

Fig. 4. **(a)** Schematic structure of metal–oxide–semiconductor (MOS) capacitors used for capacitance characterization. **(b)** Capacitance characteristics of the HZAHZO gate dielectric with various T_{OX}. Extracted **(c)** CET and **(d)** dielectric constant (k value) as a function of T_{OX}. The minimum CET achieved in this work is 1.36 nm at T_{OX} = 10 nm.

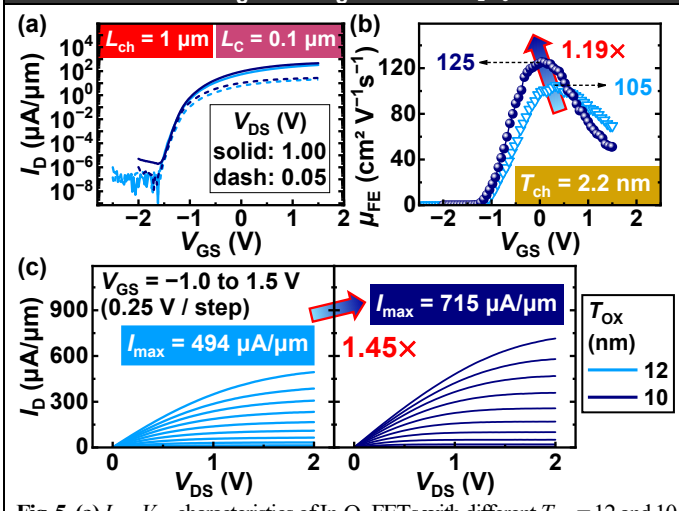

Fig. 5. **(a)** $I_D - V_{GS}$ characteristics of In_2O_3 FETs with different T_{OX} = 12 and 10 nm (CET = 1.61 and 1.36 nm) at L_{ch} = 1 μm and L_C = 0.1 μm. **(b)** μ_{FE} extracted from the $I_D - V_{GS}$ curves at V_{DS} = 0.05 V in **(a)**. **(c)** $I_D - V_{DS}$ characteristics of In_2O_3 FETs with different T_{OX} = 12 and 10 nm (CET = 1.61 and 1.36 nm).

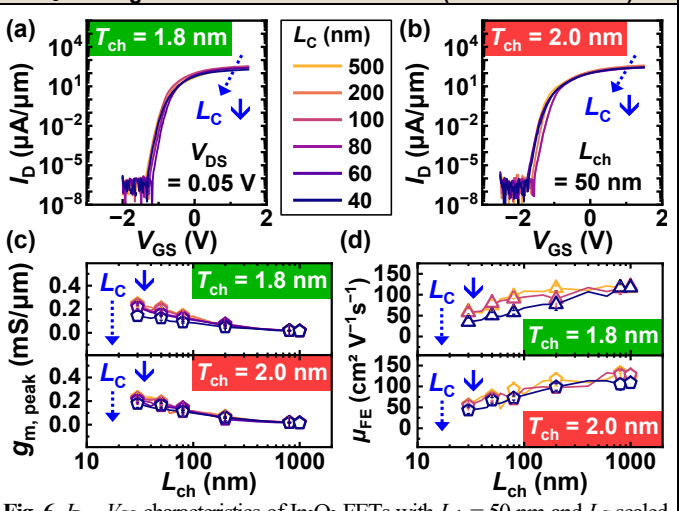

Fig. 6. $I_D - V_{GS}$ characteristics of In_2O_3 FETs with L_{ch} = 50 nm and L_C scaled from 500 nm to 40 nm for T_{ch} of **(a)** 1.8 nm and **(b)** 2.0 nm, measured at V_{DS} = 0.05 V. Extracted **(c)** $g_{m,peak}$ and **(d)** μ_{FE} as a function of L_{ch} at V_{DS} = 0.05 V, various L_C = 500 to 40 nm, and different T_{ch}.

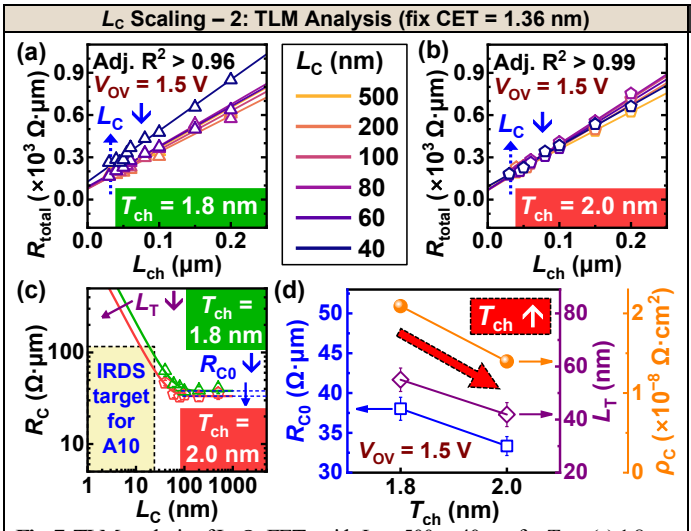

Fig. 7. TLM analysis of In_2O_3 FETs with L_C = 500 to 40 nm for T_{ch} = **(a)** 1.8 nm and **(b)** 2.0 nm, measured at V_{OV} = 1.5 V. R_{total}: total resistance. **(c)** R_C as a function of L_C, Symbols: experimental data. Solid lines: fitting curves by (1). **(d)** Extracted R_{C0}, L_T, and ρ_C obtained by fitting the $R_C - L_C$ data in **(c)** using (1) and (2).

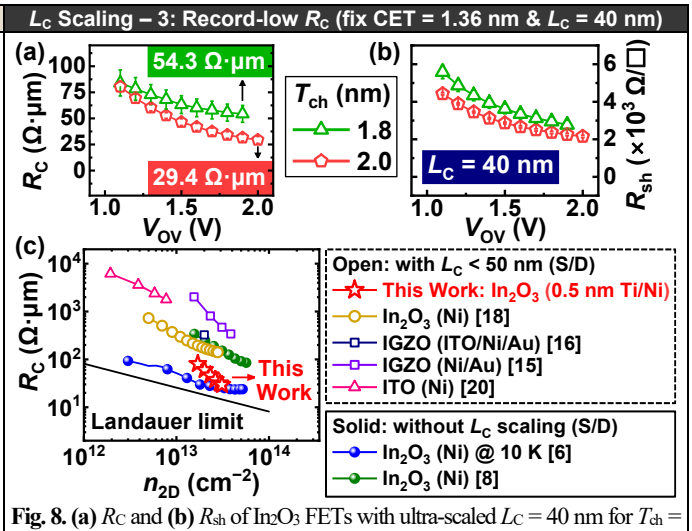

Fig. 8. (a) R_C and **(b)** R_{sh} of In_2O_3 FETs with ultra-scaled L_C = 40 nm for T_{ch} = 1.8 nm and 2.0 nm, plotted as a function of V_{OV}. **(c)** Benchmark of R_C as a function of n_{2D} for reported OS FETs. $n_{2D} = C_{OX} \cdot V_{OV} / q$, C_{OX}: gate capacitance. q: elementary charge. The devices in this work achieve a record-low R_C = 29.4 Ω·μm (extracted @ 300 K) among all OS FETs with L_C < 50 nm.

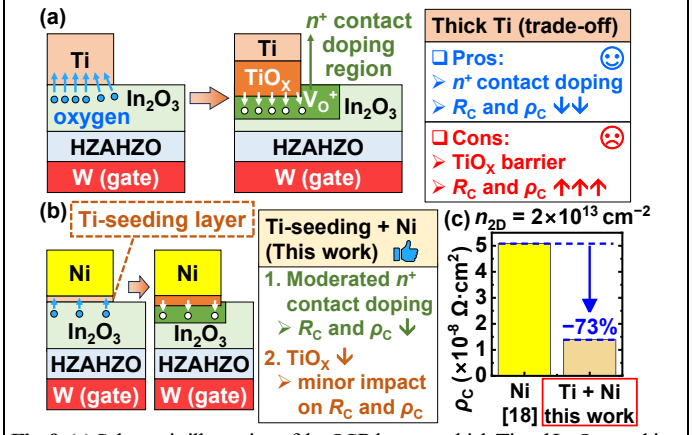

Fig. 9. (a) Schematic illustration of the OSR between thick Ti and In_2O_3, resulting in the formation of a thick interfacial TiO_X [23, 24]. Blue circle: oxygen atoms. White circle: V_O^+. n^+ indicates high electron density. **(b)** Ultrathin 0.5-nm Ti-seeding layer moderates the OSR, suppressing TiO_X thickness while maintaining n^+ contact doping. **(c)** ρ_C of In_2O_3 FETs with Ni contacts [18] and Ti-seeding layer + Ni contacts (this work). The effect of Ti work function on Φ_{SB} tuning is expected to be minor due to the non-bulk-like nature of the 0.5-nm Ti layer.

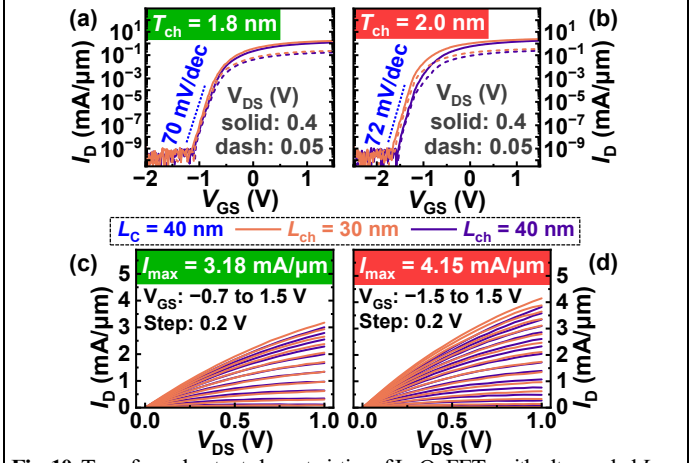

Fig. 10. Transfer and output characteristics of In_2O_3 FETs with ultra-scaled L_C = 40 nm and L_{ch} = 30 / 40 nm, corresponding to CGP = 70 / 80 nm. Devices with T_{ch} = 1.8 nm are shown in **(a)** transfer and **(c)** output curves, while those with T_{ch} = 2.0 nm are shown in **(b)** transfer and **(d)** output curves. All devices exhibit subthreshold swings (SS) below 72 mV/dec. Output characteristics are measured using pulsed $I-V$ to mitigate self-heating effects [25].

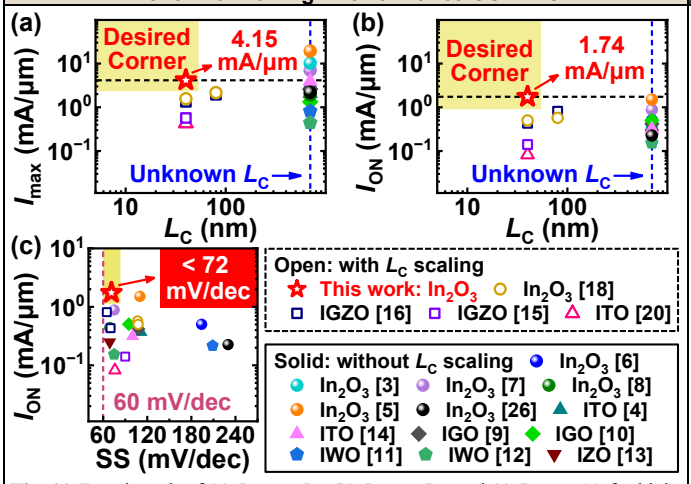

Fig. 11. Benchmark of **(a)** I_{max} vs. L_C, **(b)** I_{ON} vs. L_C, and **(c)** I_{ON} vs. SS for high-performance OS FETs, with the OS channel material indicated. I_{ON} is defined as the I_D at $V_{GS} - V_T = V_{OV} = V_{DS} = 1$ V. V_T is extracted by constant-current method at I_D/W_{ch} = 100 nA/L_{ch}. This work demonstrates record-high I_{max} = 4.15 mA/μm and record-high I_{ON} = 1.74 mA/μm among all reported OS FETs with L_C scaling.

References

[1] S. Datta *et al.*, *IEEE Micro*, 2019, doi: 10.1109/MM.2019.2942978. **[2]** K. H. Chiang *et al.*, *VLSI*, 2025, doi: 10.23919/VLSITechnologyandCir65189.2025.11074854. **[3]** Z. Lin *et al.*, *ACS Nano*, 2022, doi: 10.1021/acsnano.2c10383. **[4]** Y. Wang *et al.*, *VLSI*, 2025, doi: 10.23919/VLSITechnologyandCir65189.2025.11074860. **[5]** Z. Zhang *et al.*, *IEEE-EDL*, 2022, doi: 10.1109/LED.2022.3210005. **[6]** C. Niu *et al.*, *IEDM*, 2023, doi: 10.1109/IEDM45741.2023.10413708. **[7]** Z. Lin *et al.*, *VLSI*, 2024, doi: 10.1109/VLSITechnologyandCir46783.2024.10631497. **[8]** Y. Shao *et al.*, *IEDM*, Session 19-7, 2025. **[9]** E. Sarkar *et al.*, *IEDM*, Session 19-6, 2025. **[10]** J. Zhang *et al.*, *IEEE-TED*, 2025, doi: 10.1109/TED.2025.3583705. **[11]** E. Sarkar *et al.*, *IEDM*, 2024, doi: 10.1109/IEDM50854.2024.10873456. **[12]** H. Park *et al.*, *VLSI*, 2025, doi: 10.23919/VLSITechnologyandCir65189.2025.11075125. **[13]** Y. -K. Liang *et al.*, *VLSI*, 2023, doi: 10.23919/VLSITechnologyandCir57934.2023.10185343. **[14]** M. S. Rahman *et al.*, *IEEE-EDL*, 2025, doi: 10.1109/LED.2025.3554214. **[15]** Z. Wu *et al.*, *IEEE-EDL*, 2024, doi: 10.1109/LED.2024.3357768. **[16]** W. Zhao *et al.*, *IEDM*, 2024, doi: 10.1109/IEDM50854.2024.10873547. **[17]** S. Zhu *et al.*, *IEEE-EDL*, 2025, doi: 10.1109/LED.2025.3531420. **[18]** J. -Y. Lin *et al.*, *VLSI*, 2025, doi: 10.23919/VLSITechnologyandCir65189.2025.11074856. **[19]** J. -Y. Lin *et al.*, *IEEE-TED*, 2026, doi: 10.1109/TED.2025.3649612. **[20]** C. -H. Huang *et al.*, *IEDM*, Session 22-5, 2025. **[21]** H. Murrmann and D. Widmann, *IEEE-TED*, 1969, doi: 10.1109/T-ED.1969.16904. **[22]** J. -Y. Lin *et al.*, *IEDM*, 2024, doi: 10.1109/IEDM50854.2024.10873514. **[23]** J. -Y. Lin *et al.*, *IEEE-TED*, 2025, doi: 10.1109/TED.2025.3564265. **[24]** H. Tang *et al.*, *IEEE-TED*, 2024, doi: 10.1109/TED.2023.3332057. **[25]** P. -Y. Liao *et al.*, *IEDM*, 2022, doi: 10.1109/IEDM45625.2022.10019438. **[26]** M. Si *et al.*, *IEEE-TED*, 2021, doi: 10.1109/TED.2021.3053229.